HIP2103-4DEMO2Z Demonstration Board User Guide
3-Phase Module with HIP2103, HIP2104 Drivers

Description

The HIP2103-4DEMO2Z module is a prototyping tool that uses the HIP2103 and the HIP2104 half bridge drivers to control six on-board MOSFETs configured as a 3-phase bridge. This module is intended to drive a BLDC motor but can be used in any application that requires any combination of 3 independent half bridges.

Included in this module is a 12-pin header that interfaces control signals to the customer provided controller. Large diameter holes are also provided to connect this module to the external motor and to the high current voltage source.

The PCB layout is optimized and can be used as a guide for custom designs or it can be used as a plug-in module on the customer's controller card.

Specifications

Motor Topologies	1) 3-phase BLDC motor 2) Our bridge for brushed DC motors (bidirectional) 3) Half bridge for brushed DC motors (unidirectional)
Operating Voltage Range	5V to 40VDC
Maximum Continuous Bridge Current	60A (with sufficient air flow and/or heatsinking)
V_{CC} Output of HIP2104	3.3V ±5% at 75mA
V_{DD} Output of HIP2104	12V ±5% at 75mA

Key Features

- Small, compact 3-phase bridge module
- V_{BAT} (bridge voltage) range 5V to 40VDC
- Six high current on-board MOSFETs (60A)
- Large diameter holes for wire connections to motor and power source
- 12-pin through-hole header for signal connections to an external controller
- Clear area on the PCB backside to accommodate an optional heatsink
- Optimized PCB layout that can be used as a reference

References

- HIP2103, HIP2104 Datasheet
- AN1899, "HIP2103/HIP2104, 3-phase, Full, or Half Bridge Motor Drive User's Guide"
- UG016, "HIP2103_4DEMO3Z Demonstration Board User Guide, Full Bridge Module with HIP2103, HIP2104 Drivers"

Ordering Information

PART NUMBER	DESCRIPTION
HIP2103-4DEMO2Z	HIP2103 and HIP2104 Demonstration Board, (3-phase bridge module)

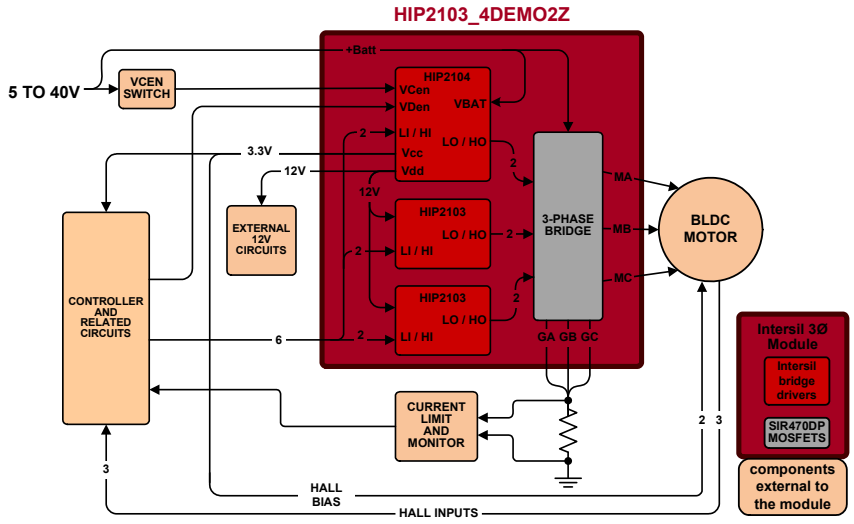

FIGURE 1. BLOCK DIAGRAM

Functional Description

This user guide covers the design details of a 3-phase bridge power module with a focus on the design implementation of the HIP2103 and HIP2104 drivers and the SIR470DP bridge MOSFETs.

This module is not a stand alone demonstration for a BLDC motor drive application. Instead, this module allows the user to quickly evaluate a 3-phase bridge application for the HIP2103 and HIP2104 using the customers controller interfaced with this module.

For an example of a demonstration board that fully implements an on-board motor controller with the HIP2103 and HIP2104 drivers and bridge MOSFETs, please refer to: AN1899 "HIP2103/HIP2104, 3-phase, Full, or Half Bridge Motor Drive User's Guide" (HIP2103_4DEMO1Z).

Included on this module are 6 MOSFETs configured as 3 half bridges. One half bridge is driven by the HIP2104 and the other two by the HIP2103s.

Two LI and HI input pairs, two inputs per half bridge, are intended to be driven by an external controller of the users choice. Also, VCen and VDen enable inputs are available to control the V_{DD} and V_{CC} regulator outputs of the HIP2104.

All boot capacitors and other necessary external parts are included in the module allowing the user to quickly apply this module to his motor drive applications with little or no changes to the module components or values.

Figure 1 illustrates one common implementation of the 3-phase bridge module to drive a BLDC motor. The external controller is the customers choice. The external current monitor and limit circuits can be implemented to control the motor torque and/or to limit the maximum currents. The on-board LDOs of the HIP2104 ($12V_{DD}$ and $3.3V_{CC}$) can optionally be used to bias external circuits.

The simplified schematic in Figure 2, illustrated the major functions of the 3-phase bridge module. Two HIP2103s and one HIP2104 half bridge drivers interface with the six 3-phase bridge MOSFETs. The MA, MB and MC outputs of the 3-phase bridge MOSFETs are the power connections to the motor. GA, GB and GC are the power ground connections of each half bridge section (the low-side bridge MOSFET sources).

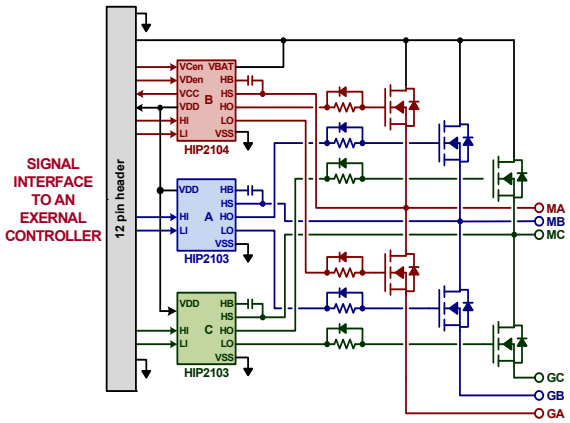

FIGURE 2. SIMPLIFIED 3-PHASE BRIDGE SCHEMATIC

Input Signals

All inputs to the HIP2103, HIP2104 drivers are compatible with 5V or 3.3V controllers. The VDen and VCen inputs (enables for V_{DD} and V_{CC}) are tolerant of voltages up to V_{BAT}. All other inputs (LI and HI) are tolerant of voltages up to V_{DD}.

Figure 1 shows six outputs from the external controller providing LI and HI inputs to the HIP2103s and HIP2104. Two inputs, VCen from the controller and VDen from an external switch, control the VCC and VDD LDOs of the HIP2104. Optionally, both VDen and VCen can be connected to the external switch or both can be connected to the external controller.

LDOs of the HIP2104

The HIP2104 (red) provides the $3.3V_{CC}$ bias for the controller and the $12V_{DD}$ bias for itself and for the two HIP2103s (blue and green). The V_{CC} and V_{DD} outputs can also be used for circuits external to the module. The total rated current of the V_{CC} output, 75mA at 3.3V, is available for external circuits. The maximum available V_{DD} current is also 75mA but is reduced by the average current for the HIP2103, HIP2104 drivers.

For a typical BLDC motor drive, for every 60° rotation, one half bridge is switching at the PWM frequency, a second half bridge is not switching but the low MOSFET is constantly on and the outputs of the third bridge are both off. Consequently, the calculation for the average gate drive for a BLDC motor driver is the current of only one half bridge.

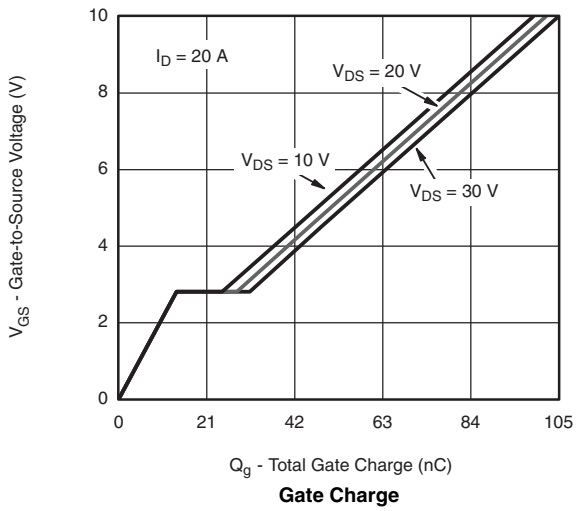

FIGURE 3. GATE CHARGE FOR THE SIR470DP BRIDGE MOSFETs

Figure 3 is used to determine the gate charge of the bridge MOSFETs.

V_{DD} from the HIP2104 is nominally 12V. Extrapolating for 12 VGS and VDS = 30V, then Q_C = 120nC. Because two MOSFETs are being driven, the average current is doubled. Assuming PWM switching freq = 20kHz then:

$$I_{gateavg} = 2Q_c \cdot freq = 4.8mA$$

The available V_{DD} current for external load, as calculated for this example is then ~70mA. The available current will be higher or lower primarily dependent on the PWM frequency used. Other applications may have higher total average gate drive current depending on the motor drive topology used, potentially two times higher.

The internal V_{DD} bias current of the drivers themselves are not significant when compared to the average gate drive current.

MOSFET Circuits

Series connected gate resistors on each bridge MOSFET are used to reduce the switching speed to help minimize EMI radiating from the power leads to the motor and to attenuate voltage transients on the PCB from parasitic inductance. The diodes in parallel with the MOSFET gate resistors are used to provide rapid turn off of the MOSFETs. The customer may change the resistor values, change the bridge MOSFETs or even remove the diodes to suit the customer's application needs.

Vishay 60A, 40V MOSFETs, are used to minimize power dissipation. With sustained total motor currents of 60A, a heatsink with an insulator can be attached to the backside of the module, if necessary.

Dead Time

The HIP2103, HIP2104 drivers do not have internal dead-time features and must be provided by the external controller. A dead time of 200ns is sufficient for the original component values on the board. Changing the gate resistors or the bridge MOSFETs may require adjustments to the dead time.

Sleep Mode

The sleep mode current (a.k.a. quiescent current) of the HIP2103, HIP2104 is invoked by setting both the LI and HI inputs to each driver high simultaneously. See Figure 4 for details to enable and disable the sleep mode. Note that SLEEP is an internal state of the driver, not an I/O.

Please refer to the HIP2103, HIP2104 datasheet for complete details.

SLEEP MODE AND NORMAL SWITCHING

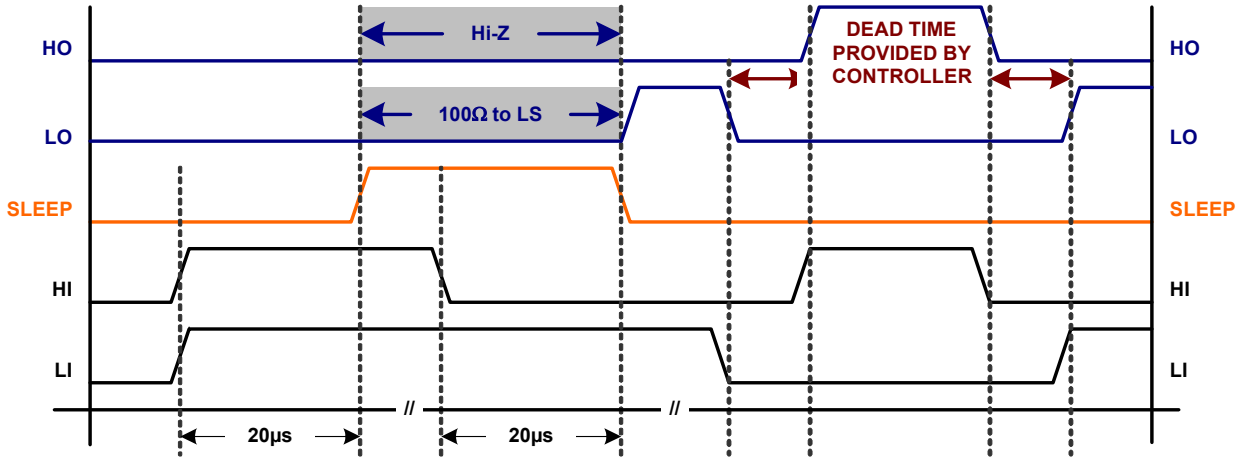

FIGURE 4. SLEEP MODE TIMING DIAGRAMS

Operating Range

Although the maximum bridge voltage for the HIP2103 and the HIP2104 is 50V, the maximum operating voltage of the 3-phase bridge module is limited to 40VDC as established by the six SIR470DP bridge MOSFETs. Because the $r_{DS(ON)}$ (2.3mΩ) of these MOSFETs is very low and because most motor driver applications switch at relatively low frequencies, it is probable that no external heatsinking will be required for most applications. If necessary, a heatsink with an insulator can be installed on the PCB side opposite the bridge MOSFETs because no components are located in this area.

PCB Layout Guidelines

The AC performance of the HIP2103, HIP2104 depends significantly on the design of the PC board. This module is intended to be used as a prototyping tool. Its main purpose is to drive a BLDC motor but can be used in other applications where half bridge MOSFETS are driven by the HIP2103, HIP2104:

- Place the driver as close as possible to the driven power MOSFET.
- Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power MOSFET will induce significant voltage transients on the associated traces.
- Keep power loops as short as possible by paralleling the source and return traces.
- Use planes where practical; they are usually more effective than parallel traces.
- Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt will induce currents and consequently, noise voltages in the low level signal lines.
- When practical, minimize impedances in low level signal circuits. Noise, magnetically induced on a 10kΩ resistor, is 10x larger than the noise on a 1kΩ resistor.
- Be aware of magnetic fields emanating from motors and inductors. Gaps in the magnetic cores of these structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling.
- The use of low inductance components such as SMT resistors and SMT capacitors is highly recommended.
- Use decoupling capacitors to reduce the influence of parasitic inductance in the V_{BAT}, V_{DD} and GND leads. To be effective, these capacitors must also have the shortest possible conduction paths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.
- It may be necessary to add resistance to dampen resonating parasitic circuits especially on LO and HO. If an external gate resistor is unacceptable, then the layout must be improved to minimize lead inductance.
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits.
- Avoid having a signal ground plane under a high amplitude dv/dt circuit. The parasitic capacitance of a ground plane, Cp, relative to the high amplitude dv/dt circuit will result in injected (Cp x dv/dt) currents into the signal ground paths.
- Do power dissipation and voltage drop calculations of the power traces. Many PCB/CAD programs have built-in tools for calculation of trace resistance. The internet is also a good source for resistance calculators for PCB trace resistance.
- Large power components (Power MOSFETs, Electrolytic caps, power resistors, etc.) have internal parasitic inductance, which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components especially parasitic inductance.

EPAD Heatsinking Considerations

The EPAD of the HIP2103, HIP2104 is electrically connected to VSS through the IC substrate. The epad has two main functions: to provide a quiet signal ground and to provide heatsinking for the IC. The EPAD must be connected to a ground plane and switching currents from the driven MOSFETs should not pass through the ground plane under the IC.

Figure 5 is a PCB layout example of how to use vias to remove heat from the IC through the EPAD.

For maximum heatsinking, it is recommended that a ground plane, connected to the EPAD, be added to both sides of the PCB. A via array, within the area of the EPAD, will conduct heat from the EPAD to the GND plane on the bottom layer. The number of vias and the size of the GND planes required for adequate heatsinking is determined by the power dissipated by the HIP2103, HIP2104, the air flow and the maximum temperature of the air around the IC.

Note that a separate plane is added under the high-side drive circuits and is connected to HS. In a manner similar to the ground plane, the HS plane provides the lowest possible parasitic inductance for the HO/HS gate drive current loop.

See the PCB layout illustrations at the end of this user guide for examples of how these guidelines for PCB layout and EPAD heatsinking are applied to the HIP2103-4DEMO2Z 3-phase bridge module.

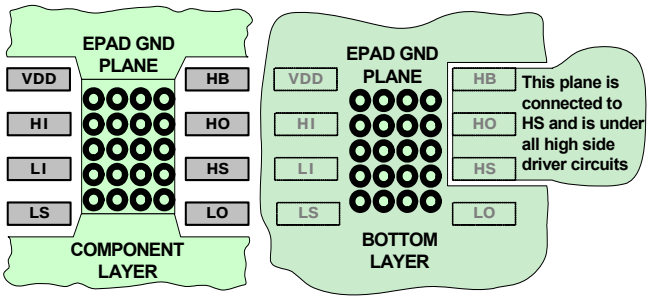

FIGURE 5. TYPICAL PCB PATTERN FOR THERMAL VIAS

Quick Start

The HIP2103-4DEMO2Z board is 1.05x1.55 inches (26.67x39.37mm). The only through-hole component is a 12-pin header with 0.1 inch centers. This header is the signal interface between the module and the external controller.

The power lead connections between the battery and the motor are 0.076 inch plated through holes large enough for 14 AWG wire.

A clear area of 0.75x1.55 inches on the non-component side of the PCB is available to mount a heatsink directly on the PCB (with insulator) should additional cooling be required.

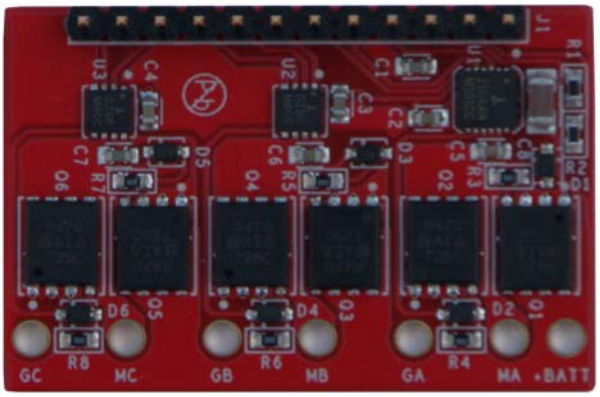

FIGURE 6. HIP2103-4DEMO2Z TOP VIEW

FIGURE 7. HIP2103-4DEMO2Z BOTTOM VIEW

Ensure that prior to start-up, that the motor leads are connected to MA, MB and MC and that the positive lead of the power source is connected to +BATT. The negative lead of the power source is connected to the users main board on the low side of the current sensing resistor(s). If no current sensing circuit is implemented (not wise), then GA, GB and GC must be connected to the negative output of the power source.

There are no start-up sequence limitations for using this board. The HIP2103, HIP2104 have built-in methods to prevent start-up problems that could be associated with random start-up of the bias voltages. However, if +BATT voltage is not present, the LDO outputs cannot be active.

It is good practice when first starting the operation of this board, to use a fan to prevent damage during prototype testing especially if the dead-time duration is not sufficient to prevent shoot-through. It is also good practice to use a regulated lab supply with adjustable current limit to help prevent damage during initial testing of the customers application.

Configuration Test

For the following test, the logic signals can be from any suitable source such as the user's microcontroller or DSP or even a logic signal generator. It is also possible to test the 3-phase module standalone, removed from the user's circuit.

To confirm the configuration of the HIP2103-4DEMO2Z in the user's custom circuit, disconnect any loads on MA, MB and MC then apply the following voltages and signals:

- +BATT = 12...40V (as required by your circuit)
- LI = HI = logic 0
- VCen = VDen = logic 1

Measure 3.3VDC on J1-4 (V_{CC}) and 12VDC on J1-7 (V_{DD}).

Now apply the LI and HI signals of Figure 8 to each half bridge driver either simultaneously or one at a time. The period of these signals can also be adjusted as required by the user's circuit. It is important to observed the 20µs start-up sequence as shown to ensure that the sleep mode is cleared.

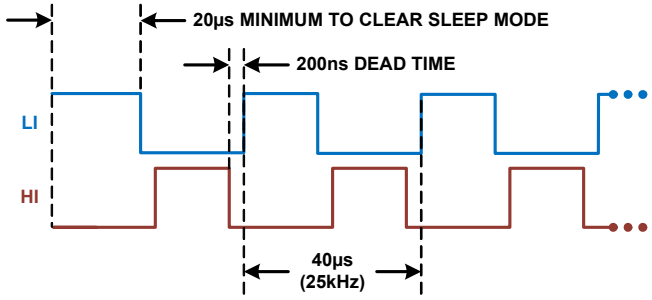

FIGURE 8. TEST SIGNALS (TIME IS NOT TO SCALE)

Figure 9 is the scope plot of the Phase A waveforms with +BATT = 20V switching at 25kHz. Similar waveforms will be observed on the other phases.

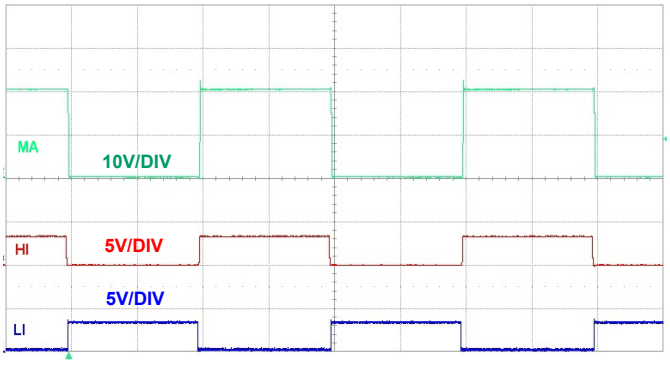

FIGURE 9. INPUT AND OUTPUT WAVEFORMS

If the MA, MB, or MC outputs are not switching when the corresponding the LI and HI inputs are active, the most likely explanation is that the drive is in sleep mode. Please refer to Figure 4 for the correct sequence to turn off or turn on the sleep mode.

PCB Design Files

The following pages contain the complete schematic and PCB layout images. The native Cadence/Orcad design files are also available for downloading from the Intersil website.

Layer 2, Layer 3 and the Bottom layer are identical. Layers 2 and 3 are provided to minimize conduction losses and to improve the thermal transfer of heat from the bridge MOSFETs to the bottom layer (on which a heatsink can be attached). If this PCB layout is used as a reference for a custom PCB, it is possible that layers two and three layers can be deleted for applications with lower sustained maximum current or with significant air flow.

Bill of materials

MANUFACTURER PART	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
HIP2103-4DEMO2ZREVBPCB	1	EA		PWB-PCB, HIP2103-4DEMO2Z, REVB, RoHS	IMAGINEERING INC
GRM188R61C105KA12D	7	EA	C1-C7	CAP, SMD, 0603, 1µF, 16V, 10%, X5R, RoHS	MURATA
C1206X7R101-105KNE	1	EA	C8	CAP, SMD, 1206, 1µF, 100V, 10%, X7R, RoHS	VENKEL
68000-236HLF	1	EA	J1	CONN-HEADER, 1x12, BRKAWY 1x36, 2.54mm, RoHS	BERG/FCI
1N4148WS-7-F	6	EA	D1-D6	DIODE-RECTIFIER, SMD, SOD-323, 2P, 75V, 150mA, RoHS	DIODES INC.
HIP2103FRTAAZ	2	EA	U2, U3	IC-60V HALF BRIDGE DRIVER, 8P, TDNF, RoHS	INTERSIL
HIP2104FRAANZ	1	EA	U1	IC-60V HALF BRIDGE DRIVER, 12P, TDFN, RoHS	INTERSIL
SIR470DP-T1-GE3	6	EA	Q1-Q6	TRANSIST-MOS, N-CHANNEL, 8P, PWRPAK, 40V, 60A, RoHS	VISHAY
CR0603-10W-36R0FT	6	EA	R3-R8	RES, SMD, 0603, 36Ω, 1/10W, 1%, TF, RoHS	VENKEL
CR0603-10W-1000FT	2	EA	R1, R2	RES, SMD, 0603, 100Ω, 1/10W, 1%, TF, RoHS	VENKEL

Schematic

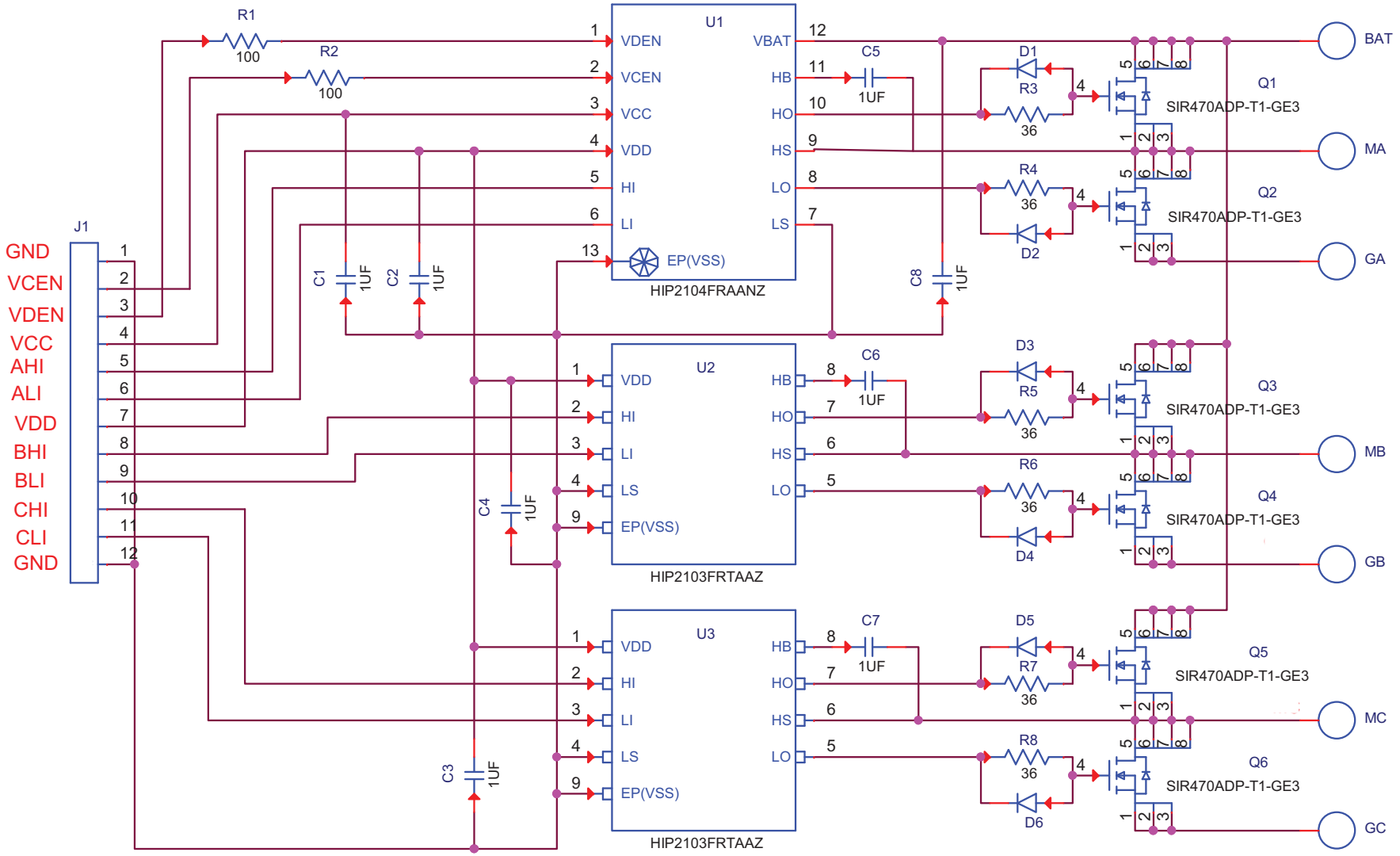

FIGURE 10. THREE-PHASE FET MODULE

Board Layout

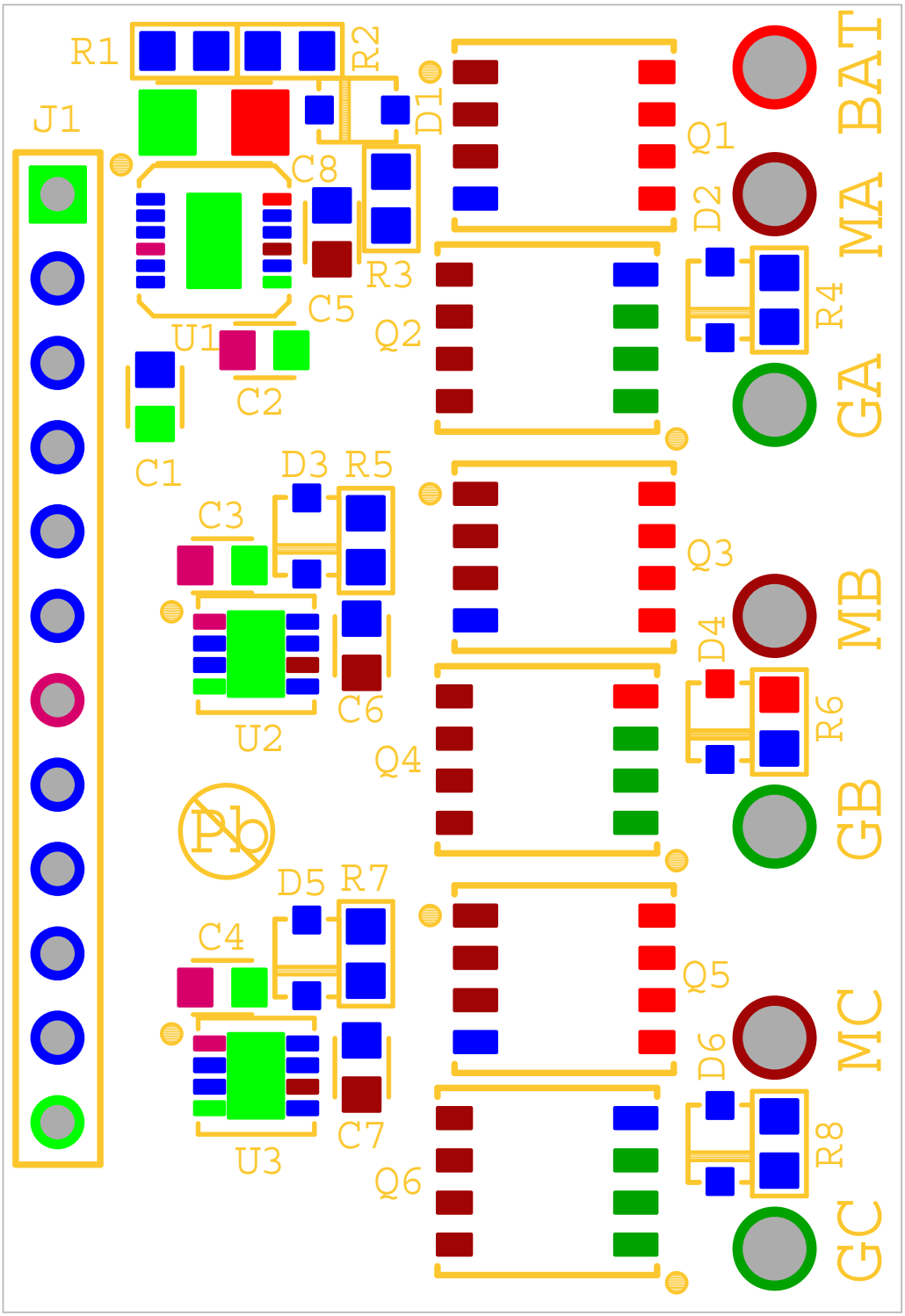

FIGURE 11. SILKSCREEN, LAYER 1 (WITH PADS)

Board Layout (Continued)

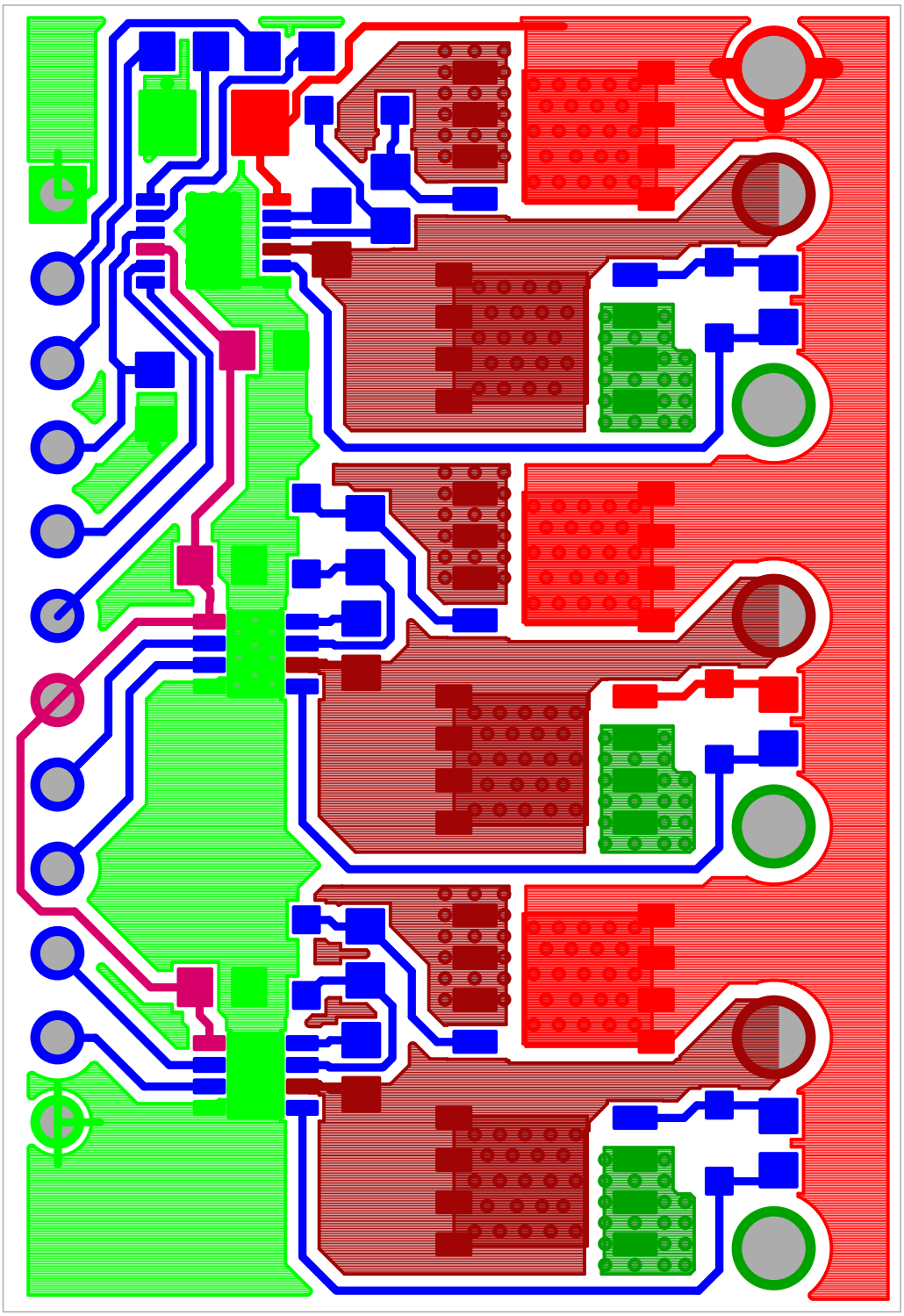

FIGURE 12. PCB, LAYER 1, COMPONENT SIDE

Board Layout (Continued)

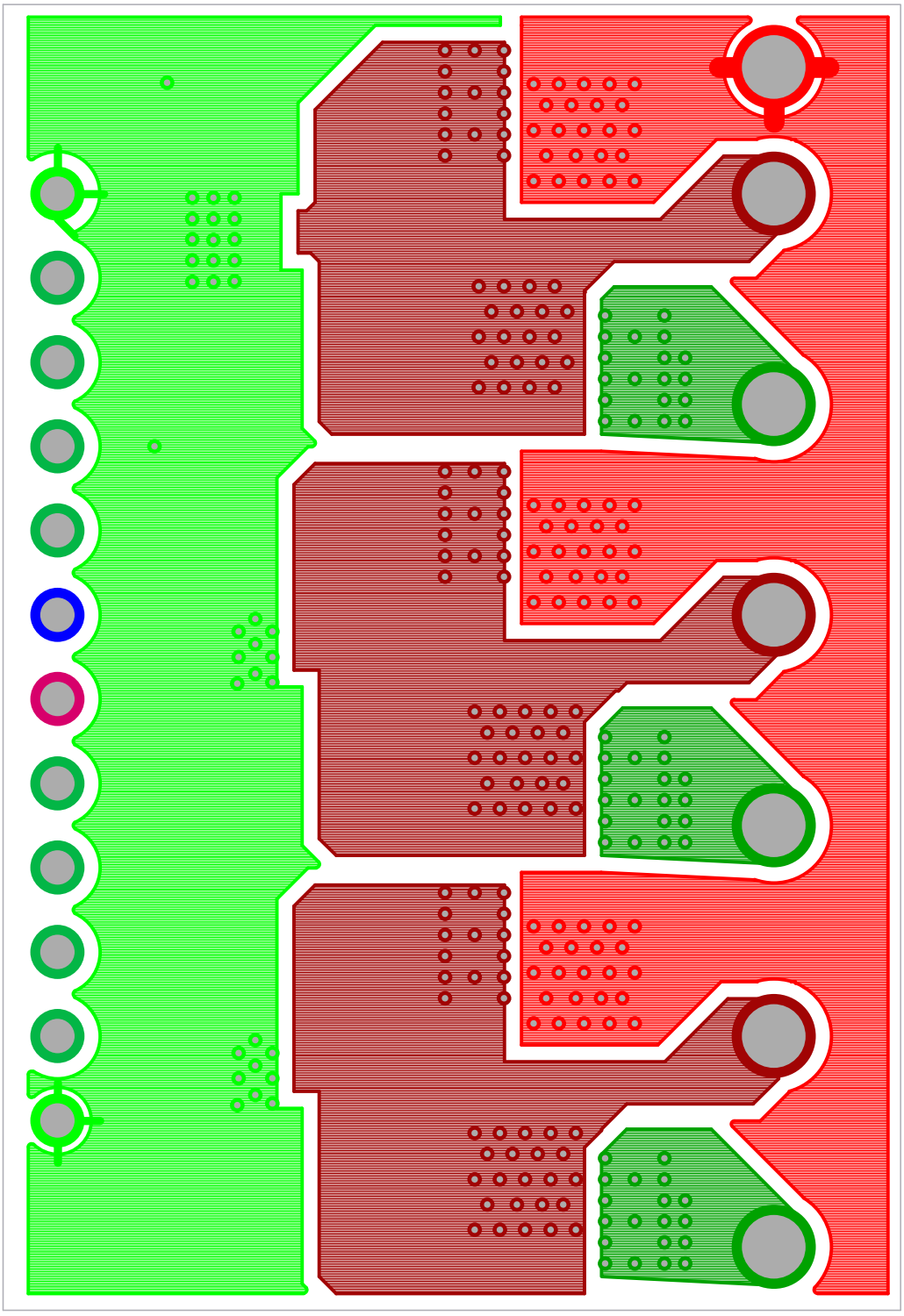

FIGURE 13. PCB, LAYER 2

Board Layout (Continued)

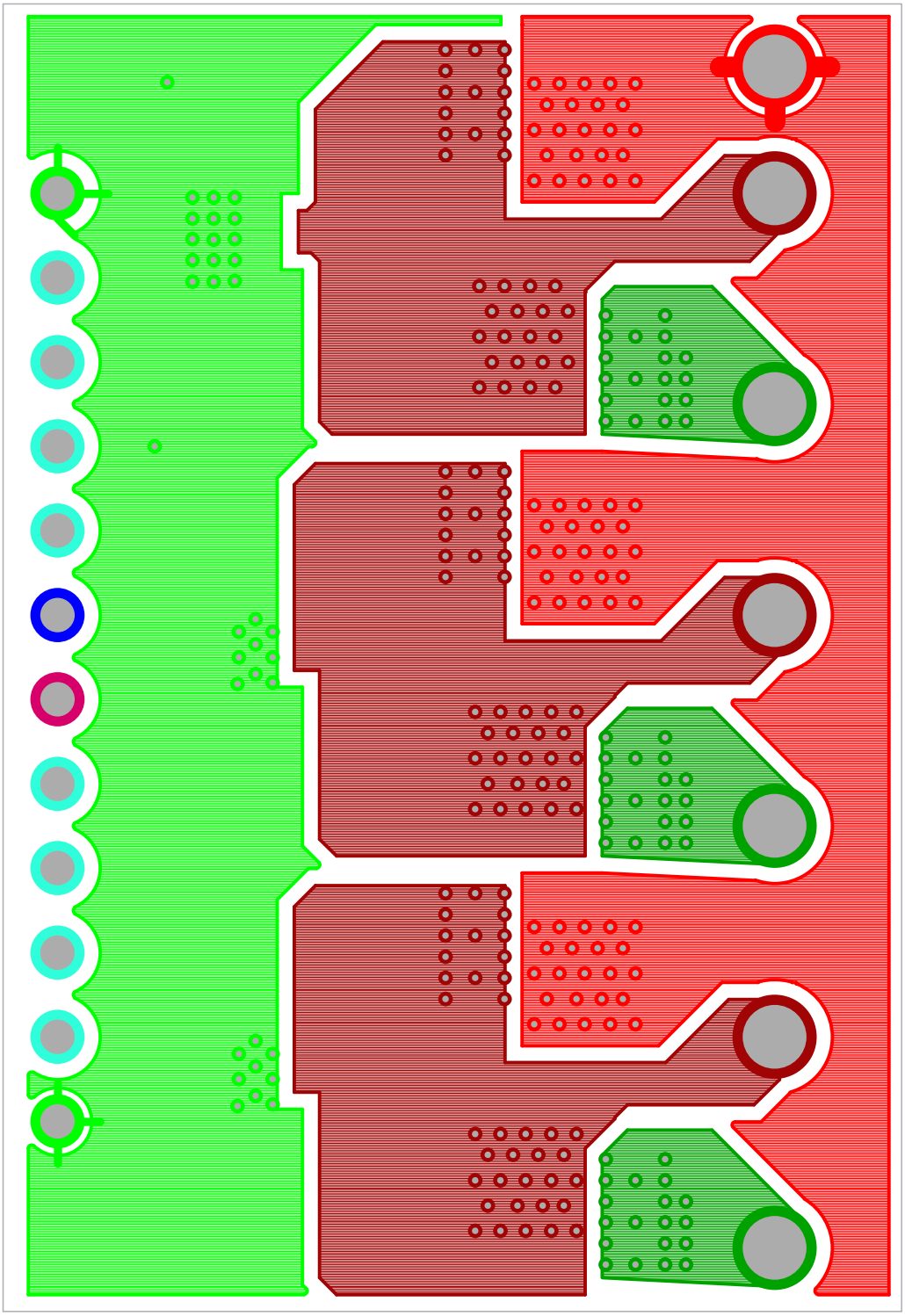

FIGURE 14. PCB, LAYER 3

Board Layout (Continued)

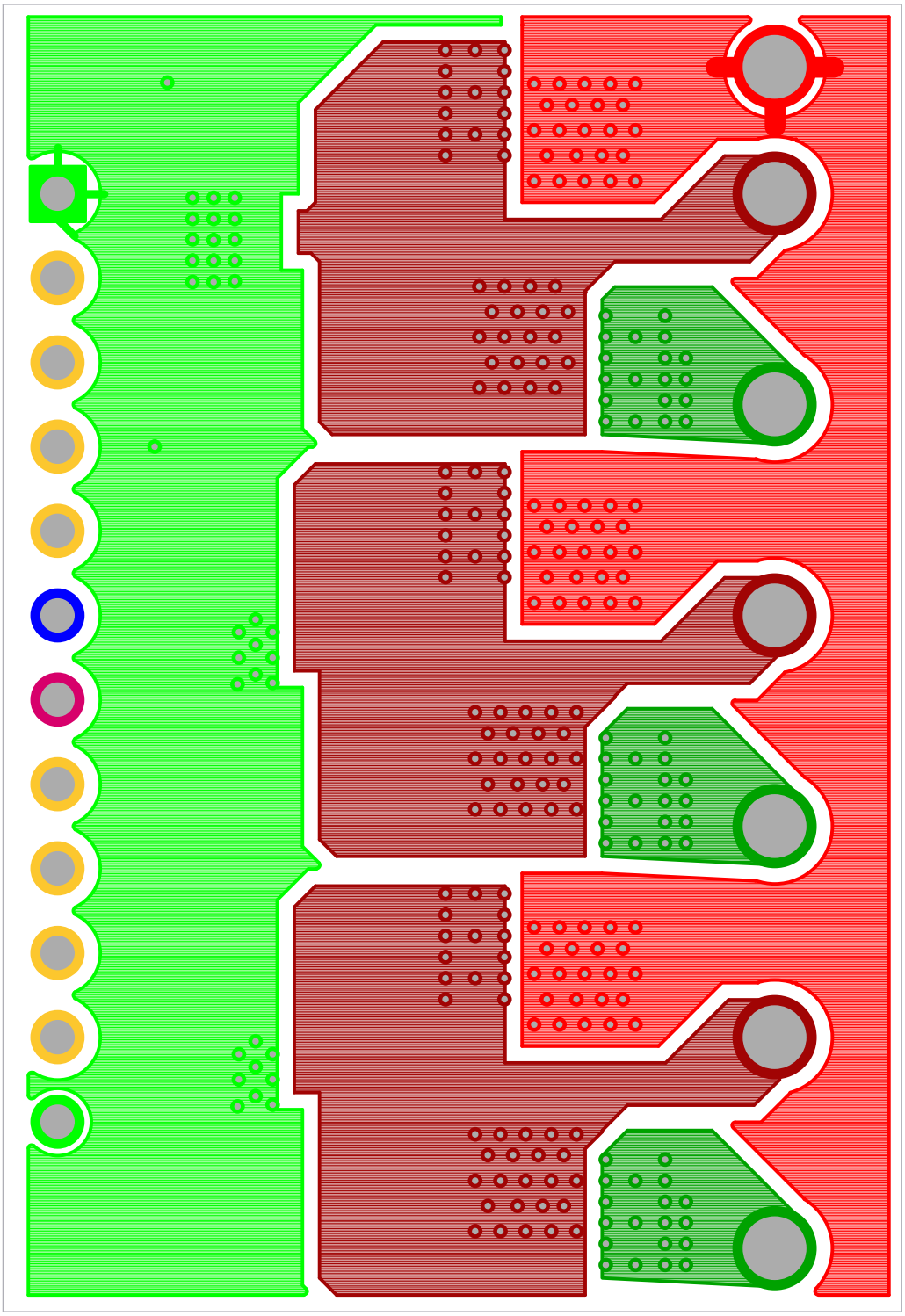

FIGURE 15. PCB, BOTTOM LAYER

Board Layout (Continued)

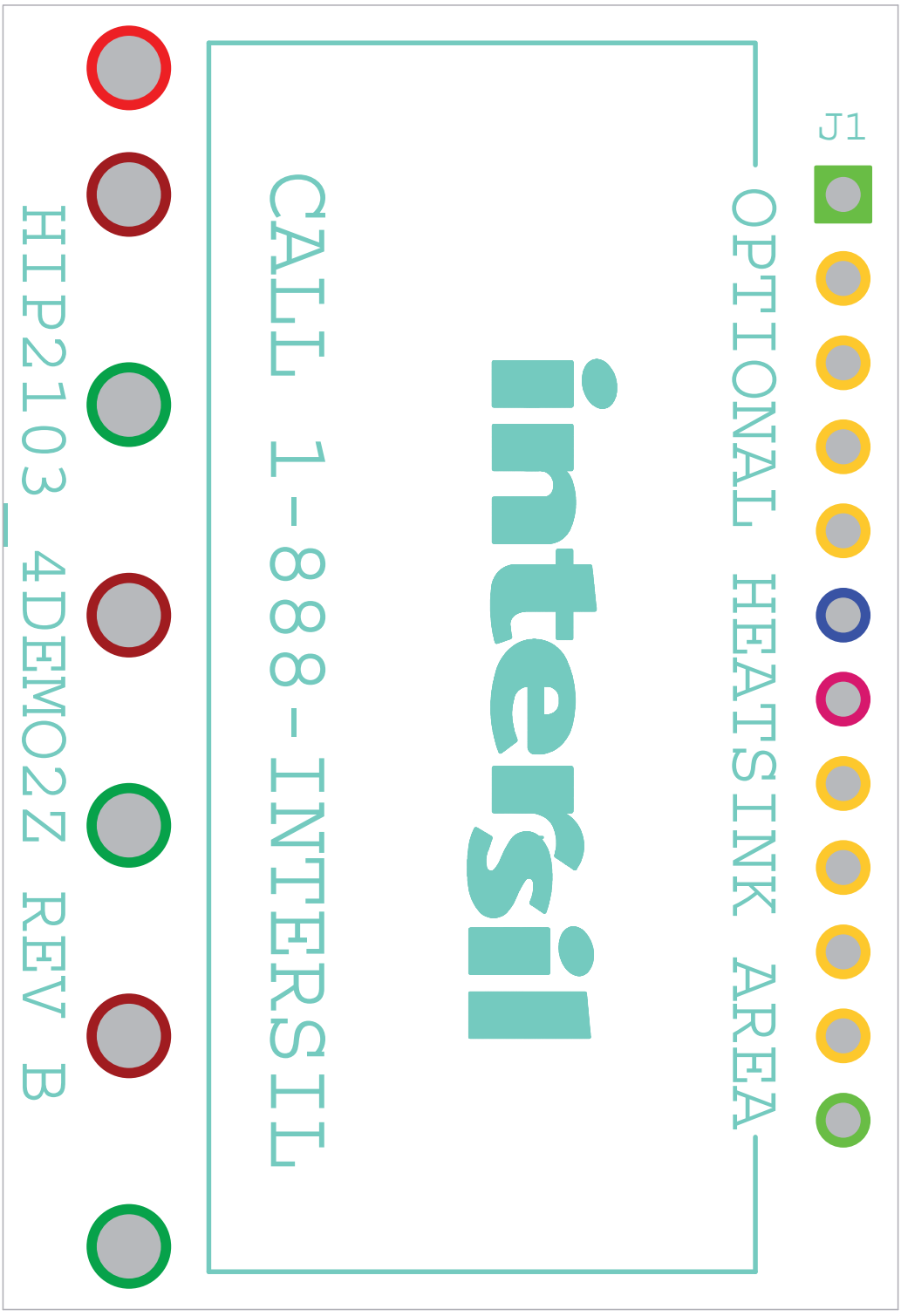

FIGURE 16. PCB, BOTTOM SILKSCREEN